

Appl. No. 10/709,026  
Amdt. dated October 11, 2007  
Reply to Office action of September 17, 2007

**Amendments to the Drawings:**

Figure 2 has been amended to change the signal at the output of OR gate 36 to read P<sub>5</sub> instead of S<sub>5</sub>. No other changes have been made. This change is fully supported by the specification, and no new matter is added.

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Acceptance of the drawings is respectfully requested.

Attachment: Replacement Sheet

1 page

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**REMARKS/ARGUMENTS**

1. Objection to claim 8:

5 Claim 8 is objected to because the claim recites "a first inverter electrically connected to a triggered end of the first flip-flop, the first inverter for inverting the target clock signal before the target clock signal is inputted to the triggered end of the *second* flip-flop" whereas Figure 2 and the specification shows that the first inverter inverts the signal before inputting to the *first* flip flop.

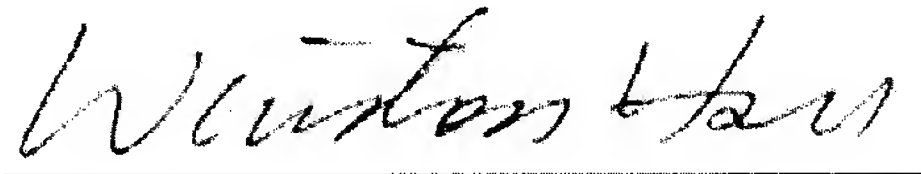
**Response:**

10 Claim 8 has been amended to make this correction, and no new matter is added.  
Acceptance of the claims is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Sincerely yours,



Date: 10.11.2007

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25 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)